WHAT IS CLAIMED IS:

1. A method of exporting from a data processor an emulation parameter value indicative of a data processing operation performed by the data processor, comprising:

providing the parameter value as a plurality of digital bits;

detecting a condition wherein the bits of a first group within the plurality of bits all have the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of the first group; and

in response to detection of said condition, outputting from the data processor via terminals thereof only the second group of bits without outputting the first group of bits.

2. The method of Claim 1, including receiving only the second group of bits externally of the data processor, and recreating the first group of bits based on the bit value of said predetermined bit.

3. The method of Claim 1, wherein the first group of bits includes at least one byte, the second group of bits includes at least one byte, and the predetermined bit is a most significant bit of said at least one byte of the second group.

4. The method of Claim 1, wherein the second group of bits includes a plurality of bytes and the predetermined bit is a most significant bit of one of the bytes of the second group.

5. The method of Claim 4, wherein said one byte of the second group is a most significant byte of the second group.

6. The method of Claim 1, wherein said emulation parameter value is a program counter value.

7. The method of Claim 1, wherein said emulation parameter value is a memory address value.

8. The method of Claim 1, wherein said emulation parameter value is a memory data value.

9. The method of Claim 1, wherein said bit value of said predetermined bit and said bits of said first group is 1.

10. The method of Claim 1, wherein said bit value of said predetermined bit and said bits of said first group is 0.

11. An integrated circuit, comprising:

a data processor for performing data processing operations;

a plurality of terminals for outputting information;

an apparatus for exporting from said integrated circuit an emulation parameter value indicative of a data processing operation performed by said data processor, including an input coupled to said data processor for receiving said parameter value as a plurality of digital bits;

said apparatus including an evaluator coupled to said input for detecting a condition wherein the bits of a first group within the plurality of bits all have the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of said first group, said evaluator operable for providing condition information which indicates that said condition has been detected; and

said apparatus including a compression determiner coupled to said evaluator and said terminals and said input, said compression determine responsive to said condition information for outputting via said terminals only the second group of bits without outputting the first group of bits.

12. The integrated circuit of Claim 11, wherein the first group of bits includes at least one byte, the second group of bits includes at least one byte, and the predetermined bit is a most significant bit of said at least one byte of the second group.

13. The integrated circuit of Claim 11, wherein the second group of bits includes a plurality of bytes and the predetermined bit is a most significant bit of one of the bytes of the second group.

14. The integrated circuit of Claim 13, wherein said one byte of the second group is a most significant byte of the second group.

15. The integrated circuit of Claim 11, wherein said emulation parameter value is one of a program counter value, a memory address value and a memory data value.

16. The integrated circuit of Claim 11, wherein said bit value of said predetermined bit and said bits of said first group is 1.

17. The integrated circuit of Claim 11, wherein said bit value of said predetermined bit and said bits of said first group is 0.

18. A data processing system, comprising:

an integrated circuit, including a data processor for performing data processing operations;

an emulation controller coupled to said integrated circuit for controlling emulation operation of said data processor;

said integrated circuit including an apparatus coupled between said data processor and said emulation controller for exporting from said integrated circuit an emulation parameter value indicative of a data processing operation performed by said data processor, said apparatus including an input coupled to said data processor for receiving said parameter value as a plurality of digital bits;

said apparatus including an evaluator coupled to said input for detecting a condition wherein the bits of a first group within the plurality of bits all have the same bit value and a predetermined bit within a second group of the plurality of bits has a bit value equal to the bit value of the bits of said first group, said emulator operable for providing condition information which indicates that said condition has been detected; and

said integrated circuit including a plurality of terminals coupled to said emulation controller for outputting information to said emulation controller, and said apparatus

including a compression determiner coupled to said evaluator and said terminals and said input, said compression determiner responsive to said condition information for outputting to said emulation controller, via said terminals, only the second group of bits without outputting the first group of bits.

19. The system of Claim 18, including a man/machine interface coupled to said emulation controller for permitting a user to communicate with said emulation controller.

20. The system of Claim 19, wherein said man/machine interface includes one of a visual interface and a tactile interface.